**QB.COA-M2**

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**Q1**. **Explain various Instruction Formats.**

Types of Instruction Formats

Depending on the number of address fields, instructions are classified as:

1. Zero-Address Instructions

Used in stack-based architectures.

No explicit operand address is given.

Operands are implicitly on top of the stack.

Example:

PUSH A

PUSH B

ADD ; pops A & B, pushes result

2. One-Address Instructions

Uses a single address field.

An Accumulator (AC) is used implicitly.

Example:

ADD X → AC ← AC + M[X]

3. Two-Address Instructions

TwO operands are explicitly mentioned.

Usually, one operand also serves as the destination.

Example:

ADD R1, R2 → R1 ← R1 + R2

4. Three-Address Instructions

Explicitly specifies two source operands and one destination.

Example:

ADD R1, R2, R3 → R1 ← R2 + R3

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**Q2.** **Draw and Explain Basic Instruction Cycle with Interrupt Processing.**

Basic Instruction Cycle with Interrupt Processing

Instruction Cycle

A program residing in the memory unit of the computer consists of a sequence of instructions.

The program is executed in the computer by going through a cycle for each instruction.

Each instruction cycle in turn is subdivided into a sequence of sub-cycles or phases.

Instruction Cycle:

In the basic computer each instruction cycle consists of the following phases:

Fetch an instruction from memory

2. Decode: Decode the instruction Decode

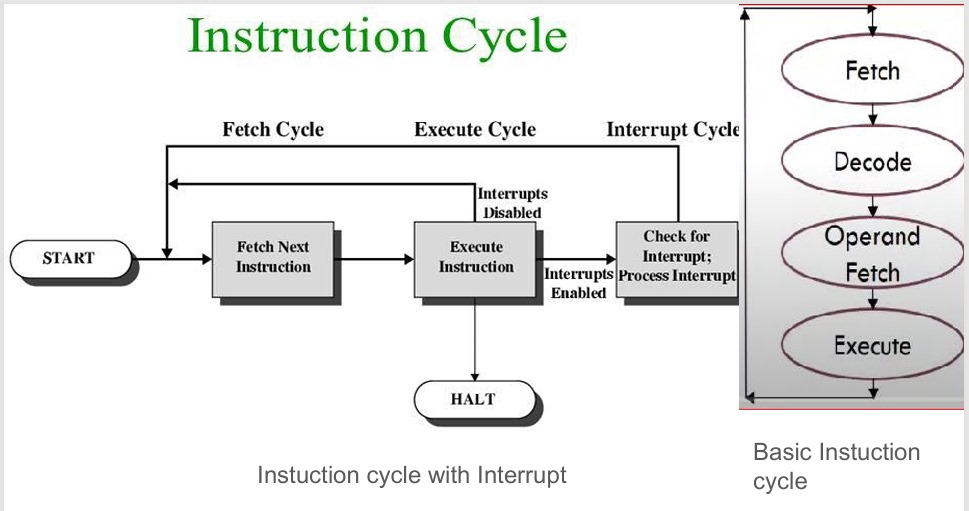
3. Operand Fetch: Read the effective address from memory if the instruction has a indirect address Operand

4. Execute: Execute the instruction

Upon the completion of step 4, the control goes back to step I to fetch, decode and execute the next instruction.

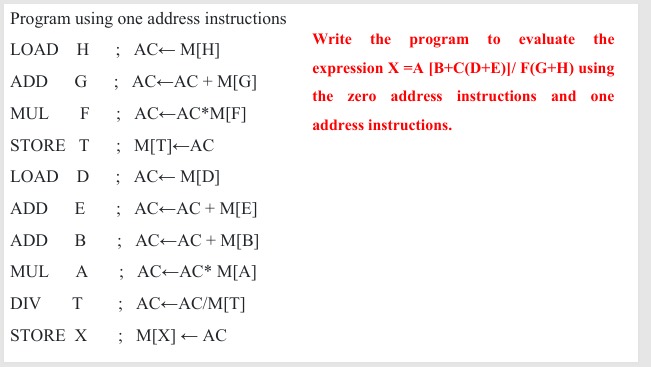
This process continues indefinitely unless a HALT instruction is encountered.

To perform fetch, decode and execute cycles the processor has to perform set of microperations.



**3. Given X =A [B+C(D+E)]/ F(G+H) Write the program to evaluate the expression ,**

**using the one address instructions.**

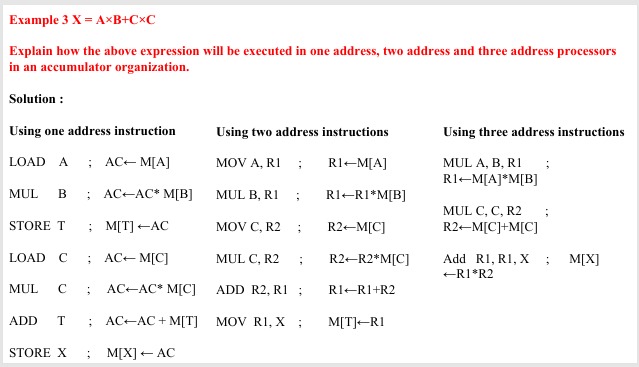


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**4. Example :X = A×B+C×C**

**Explain how the above expression will be executed in one address, two address**

**and three address processors in an accumulator organization**.

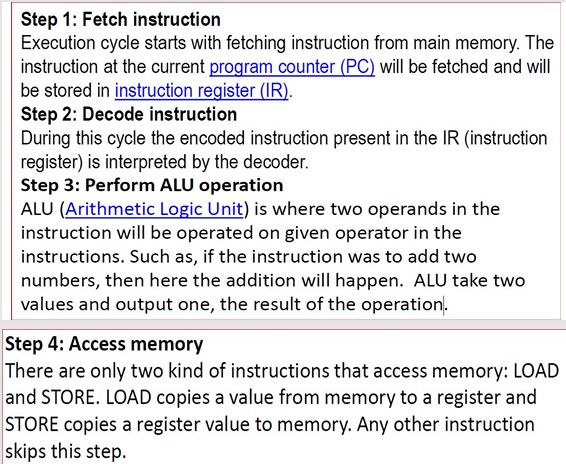


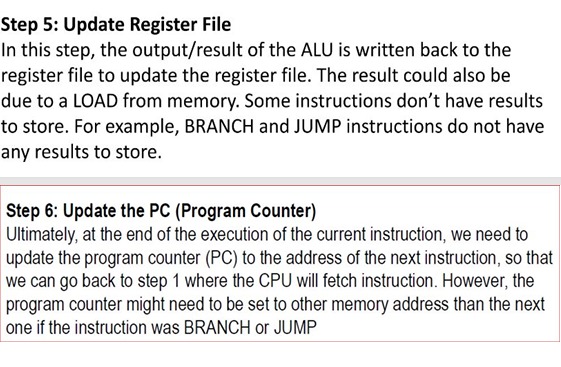
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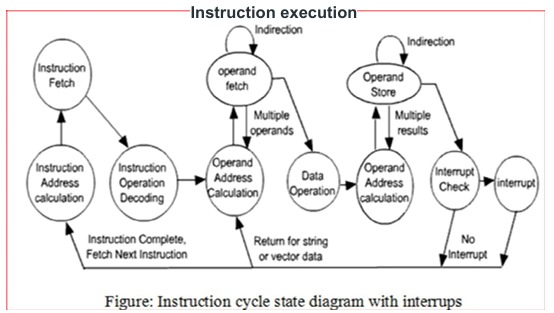
**5. What are the stages involved in the Basic Instruction Cycle explain in detail with**

**diagram.**

**STAGES INVOLVED IN THE BASIC INTRUCTIONS CYCLES ARE=**

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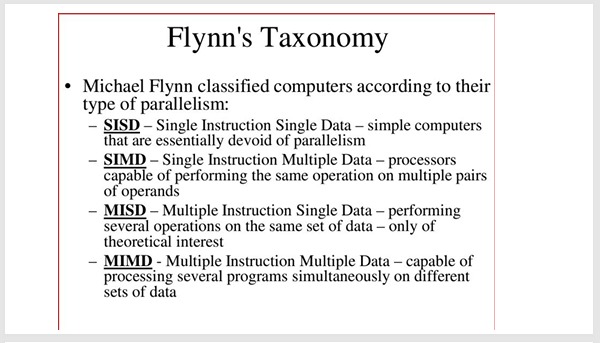
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**6. Briefly illustrate the instruction cycle state diagram with interrupts.**

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**Q7.** **Explain Flynn’s Classifications, in detail.**

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The SISD is a traditional uniprocessor. There is a single control unit and a single execution

unit. Hence, it has one instruction and one data stream.

● The SIMD has one control unit that handles multiple execution units. Each execution unit

has a separate data stream.

● The MISD involves multiple control units but a single execution unit. Such a system is not

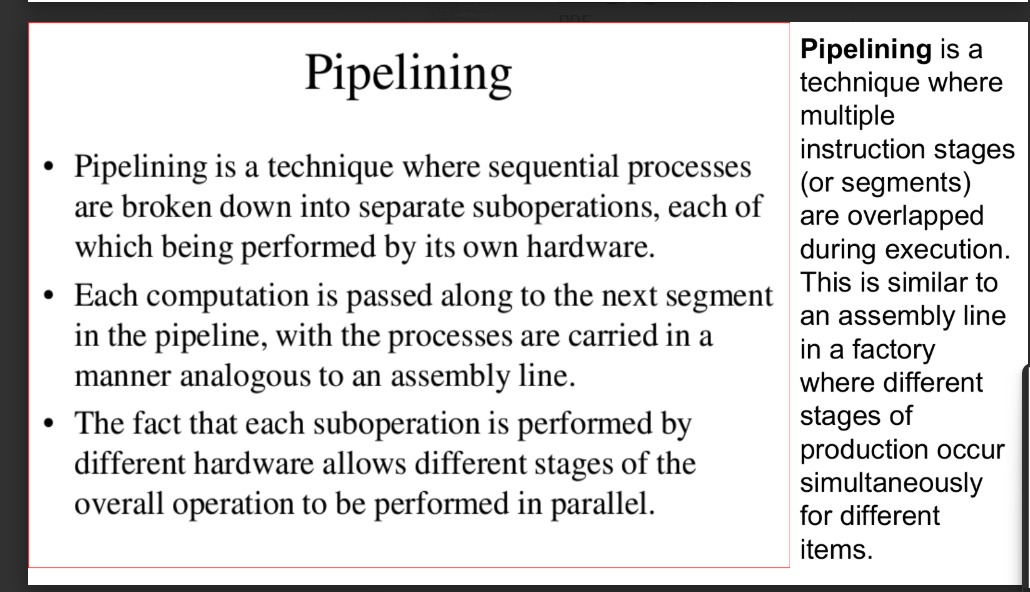
practically feasible.

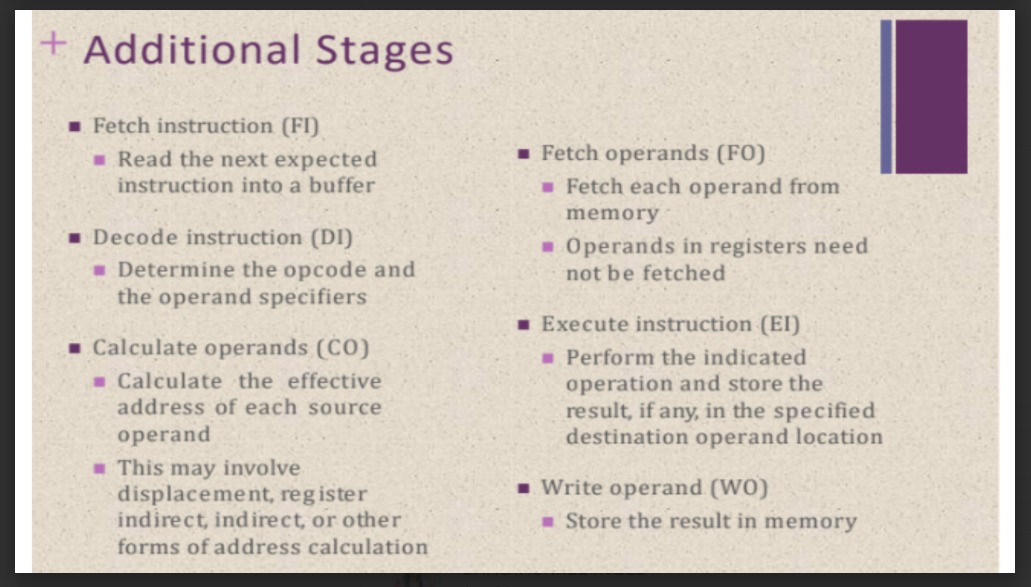
● The MIMD refers to multiple control units and multiple execution units. Multiprocessors

and parallel processors are examples of this type.

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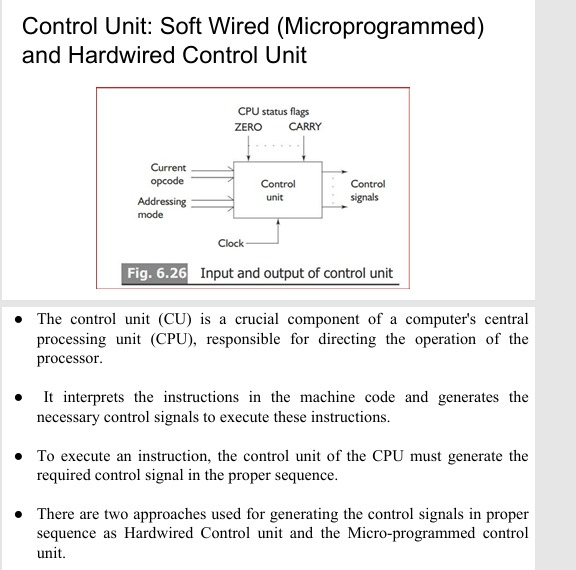
**9**. **Illustrate the 6 stage Pipelining**.



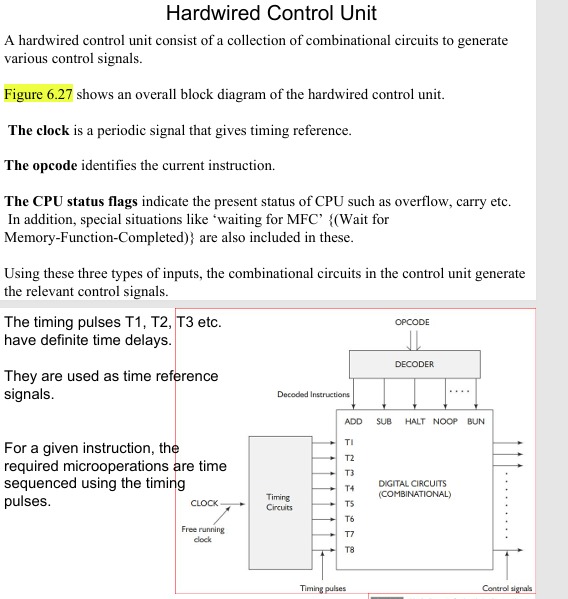


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**10. Explain the Control Unit: Soft Wired (Micro programmed).**

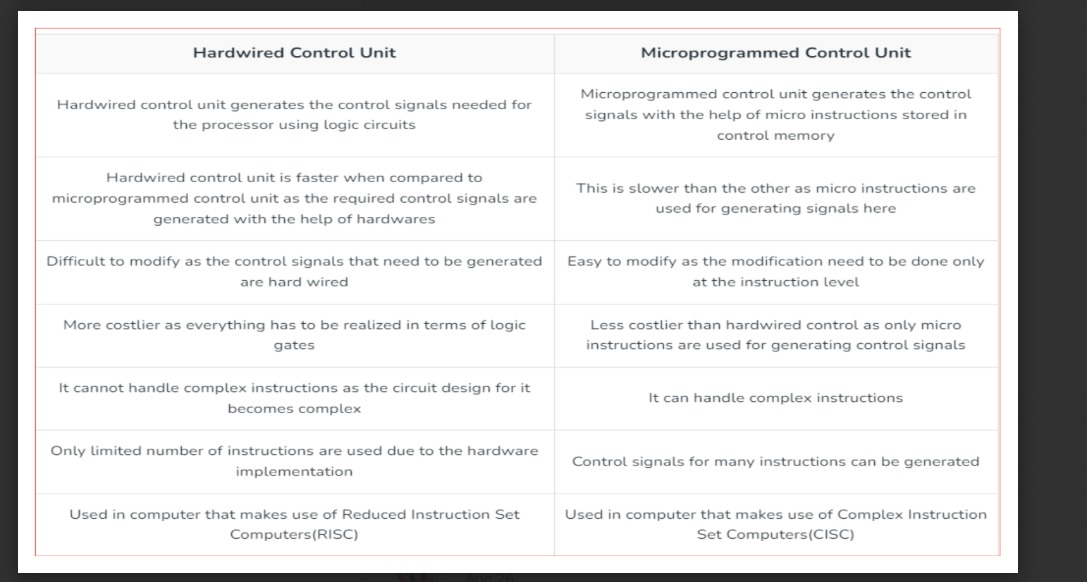
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**11.Explain the Control Unit: Hardwired Control Unit.**

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**12. State the difference between Soft wired and Hardwired Control units.**

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